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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. 0756-1984

First Inventor or Application Identifier: Shunpei YAMAZAKI et al.

Title: SEMICONDUCTOR DEVICE AND FABRICATION METHOD
THEREOF

Express Mail Label No.

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO:

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1. ☒ Fee Transmittal Form (e.g., PTO/SB/17)
(Submit an original, and a duplicate for fee processing)
2. ☒ Specification Total Pages [40]
(preferred arrangement set forth below)
 - Descriptive title of the invention
 - Cross References to Related Applications
 - Statement Regarding Fed sponsored R & D
 - Reference to Microfiche Appendix
 - Background of the Invention
 - Brief Summary of the Invention
 - Brief Description of the Drawings (if filed)
 - Detailed Description
 - Claim(s)
 - Abstract of the Disclosure
3. ☒ Drawing(s) (35 USC 113) Total Sheets [8]
4. ☒ Oath or Declaration Total Pages [2]
 - a. ☐ Newly executed (original or copy)
 - b. ☒ Copy from a prior application (37 CFR 1.63(d))
(for continuation/divisional with Box 17 completed)
[Note Box 5 below]
 - i. ☐ **DELETION OF INVENTOR(S)**
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. ☒ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ☐ Microfiche Computer Program (Appendix)
7. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
 - a. ☐ Computer Readable Copy
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 - c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ☐ Assignment Papers (cover sheet & document(s))
9. ☐ 37 CFR 3.73(b) Statement ☐ Power of Attorney
(when there is an assignee)
10. ☐ English Translation Document (if applicable)
11. ☒ Information Disclosure Statement ☐ Copies of IDS
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17. If a **CONTINUING APPLICATION**, check appropriate box, and supply the requisite information below and in a preliminary amendment
- Divisional of prior application Serial No. 08/938,310, filed September 26, 1997; which itself is a Division of application Serial No. 08/513,090, filed August 9, 1995, now U.S. Patent No. 5,731,613.
- Prior application information: Examiner: F. Abraham Group/Art Unit: 2811

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Date: June 17, 1999

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT Application of)
Shunpei YAMAZAKI et al.)
Based On Serial No. 08/938,310) Art Unit: 2811
Which Was Filed: September 26, 1997) Examiner: F. Abraham
For: SEMICONDUCTOR DEVICE AND)
FABRICATION METHOD)
THEREOF) Date: June 17, 1999

NOTICE OF CHANGE OF ADDRESS

Honorable Assistant Commissioner for Patents

Washington, D.C. 20231


Sir:

Effective immediately, please note that the address of the attorney(s) of record in the above-referenced application has been changed. Please direct all future correspondence to:

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Respectfully submitted,



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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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For: SEMICONDUCTOR DEVICE AND)
FABRICATION METHOD)
THEREOF) Date: June 17, 1999

PRELIMINARY AMENDMENT

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Please preliminarily amend the subject application as follows:

IN THE SPECIFICATION:


Before the first sentence of the specification, insert --This application is a Division of application Serial No. 08/938,310, filed September 26, 1997; which itself is a Division of application Serial No. 08/513,090, filed August 9, 1995, now U.S. Patent No. 5,731,613--.

REMARKS

This application has been amended to include the continuing application data thereof.

Examination on the merits is requested.

Respectfully submitted,



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654790-9110-8494660

TITLE OF THE INVENTION

Semiconductor device and fabrication method thereof

BACKGROUND OF THE INVENTION

Description of the related art

In recent years research has been conducted into techniques for forming transistors which employ thin-film semiconductors on a glass or quartz substrate (referred to as thin-film transistors). In particular, techniques employing amorphous silicon as the thin-film semiconductor have been put to practical use, for use in active matrix-type liquid crystal display devices and the like.

However, thin-film transistors which employ amorphous silicon have the problem that their characteristics are poor. For example, if an improvement is required in the display function of an active matrix-type liquid crystal display device, the characteristics of thin-film transistors which employ amorphous silicon are too poor to achieve this.

Further, techniques are known for constructing thin-film transistors using crystalline silicon films in which amorphous silicon films have been crystallized. These techniques involve transforming an amorphous silicon film into a crystalline silicon film by performing heat treatment or irradiation with laser light after formation of the amorphous silicon film. Crystalline silicon films obtained by crystallizing amorphous silicon films generally have a multicrystalline construction or a microcrystalline construction.

By constructing thin-film transistors using crystalline silicon films it is possible to obtain much better characteristics than if amorphous silicon films are used. For example, considering the mobility, which is one index with which to evaluate the characteristics of thin-film

transistors, with thin-film transistors employing amorphous silicon films the mobility is $1 \text{ cm}^2/\text{Vs}$ or less, but with thin-film transistors employing crystalline silicon films, a value of approximately $100 \text{ cm}^2/\text{Vs}$ can be achieved.

However, crystalline silicon films which are obtained by crystallizing amorphous silicon films have a multicrystalline construction, and there are a number of problems which result from crystal grain boundaries. For example, since some carriers migrate via crystal grain boundaries, there is the problem that voltage resistance is greatly limited. There is the further problem that under high speed operation, for example, variation and degradation of the characteristics is liable to occur. There is furthermore the problem that since some carriers migrate via crystal grain boundaries, there is a large leak current when the thin-film transistor is off.

Further, in order to construct active matrix-type liquid crystal display devices in a more integrated fashion it is desirable to form not only the pixel region but also the peripheral circuitry on a single glass substrate. In such cases the thin-film transistors which are arranged in the peripheral circuitry must be able to handle large currents in order to drive the many thousands of pixel transistors which are arranged in matrix form.

In order to obtain thin-film transistors which can handle large currents it is necessary to adopt a construction which has a wide channel. However, with thin-film transistors which employ polycrystalline silicon films or microcrystalline silicon films there is a problem that this cannot be realized even if the channel is widened, due to the problem of voltage resistance. There is the further problem that variations in the threshold voltage and the like are large, and they are therefore not practical.

SUMMARY OF THE INVENTION

The invention disclosed in the present specification aims to provide a thin-film transistor which is not affected by crystal grain boundaries.

Further, another aim of the invention disclosed in the present invention is to provide a thin-film transistor which has a large voltage resistance and with which it is possible to handle large currents.

Further, yet another object of the invention disclosed in the present specification is to provide a thin-film transistor with which there is no degradation or variation in the characteristics.

One invention disclosed in the present specification is a semiconductor device which employs a thin-film silicon semiconductor which is formed on a substrate which has an insulating surface, wherein

the abovementioned thin-film silicon semiconductor has a region which can be regarded as being effectively monocrystalline,

the abovementioned region constitutes at least part of an active layer,

and the abovementioned region contains carbon and nitrogen atoms at a concentration of between $1 \times 10^{16} \text{ cm}^{-3}$ and $5 \times 10^{18} \text{ cm}^{-3}$, oxygen atoms at a concentration of between $1 \times 10^{17} \text{ cm}^{-3}$ and $5 \times 10^{19} \text{ cm}^{-3}$, and hydrogen atoms, which neutralize the unpaired bonds in the silicon, at a concentration of between $1 \times 10^{17} \text{ cm}^{-3}$ and $5 \times 10^{20} \text{ cm}^{-3}$.

With the abovementioned construction, a region which can be regarded as being effectively monocrystalline refers to a thin-film silicon semiconductor region which has a crystalline construction which is taken to be equal to the crystallinity of a monocrystalline silicon wafer. Specifically, a region which is regarded as being

effectively monocrystalline is defined as being a region in which the Raman spectrum intensity ratio in comparison with the Raman spectrum for monocrystalline silicon is at least 0.8, the ratio of the full-widths at half magnitude (relative values) is 2 or less, and at the same time there are effectively no crystal grain boundaries in said region.

Such a region which can be regarded as being effectively monocrystalline can be obtained using an amorphous silicon film as the starting film, and heating it or irradiating it with laser light. In particular, by introducing metal elements which promote crystallization of the silicon, it is possible to obtain the abovementioned region which can be regarded as being effectively monocrystalline, relatively easily over a large area.

One or more elements selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, Zn, Ag and Au can be used as the metal elements which promote crystallization of the silicon. These elements have the property that they penetrate into silicon, and they disperse within the silicon film when heat treatment or irradiation with laser light is effected. From among the abovementioned elements, Ni (nickel) is an element with which it is possible to obtain particularly striking effects.

It is important for the abovementioned metal elements to be contained in the final silicon film after completion of crystallization at a concentration of between 1×10^{16} and $5 \times 10^{19} \text{ cm}^{-3}$. If the concentration of the metal elements is less than $1 \times 10^{16} \text{ cm}^{-3}$ then it is not possible to obtain crystallization-promoting effects, and if the concentration is more than $5 \times 10^{19} \text{ cm}^{-3}$ then the quality of the semiconductor is impaired.

The following methods can be used to form the region which can be regarded as being effectively monocrystalline

within the silicon thin film. Firstly, an amorphous silicon film is formed on a glass substrate or a quartz substrate, after which a film containing nickel is formed on the surface of the amorphous silicon film. The film containing nickel may be one in which an extremely thin nickel film is formed by the sputtering method, for example, or a method may be adopted whereby the nickel element is disposed in contact with the surface of the amorphous silicon film by applying a solution containing nickel onto the surface of the amorphous silicon film.

Having introduced the nickel element into the amorphous silicon film the amorphous silicon film is crystallized by being heat treated. This heat treatment may be performed at a temperature of 600°C or less due to the action of the nickel element. If a glass substrate is used as the substrate then it is preferable for the temperature of the heat treatment to be as low as possible, but in consideration of the efficiency of the crystallization process it is advantageous for the temperature to be 500°C or more, preferably 550°C or more. It should be noted that when a quartz substrate is used for the substrate, the heat treatment may be performed at a temperature of 800°C or more, and it is possible to obtain a crystalline silicon film in a short time. The crystalline silicon film obtained by this process has a multicrystalline or microcrystalline form, and there are crystal grain boundaries within the film.

Then, by irradiating the sample with laser light, with the sample heated to a temperature of 450°C or more, crystallization is promoted locally. By this process it is possible to form a region which can be regarded as being monocrystalline. When the laser light is being irradiated, it is important to heat the sample or the irradiated surface

to a temperature of 450°C or more. The heating temperature is preferably between 450°C and 750°C, and in particular, when a glass substrate is being used as the substrate, between 450°C and 600°C.

Further, another method which can be cited as a method for forming the region which can be considered to be monocrystalline is one in which an amorphous silicon film is formed, a metal element which promotes crystallization is introduced, and the region which can be considered to be monocrystalline is formed by irradiating with laser light without performing heat treatment. In this case also it is important to heat the sample to between 450°C and 750°C during the irradiation with laser light, and in particular if a glass substrate is being used for the substrate, to heat it to a temperature of between 450°C and 600°C.

The significance of heating the sample during irradiation with laser light will now be explained. Figure 4 shows the Raman spectrum intensity when laser light is irradiated onto an amorphous silicon film in which a base silicon oxide film has been formed on a glass substrate, an amorphous silicon film has been formed thereon and nickel element has been introduced onto the surface thereof. Further, each plotted point indicates the temperature to which the sample was heated when the laser light was irradiated.

The Raman intensities shown in Figure 4 are relative values showing the ratio (I/I_0) between the Raman spectrum intensity I_0 of a monocrystalline silicon wafer and the Raman spectrum intensity I of the sample. The Raman spectrum intensity is defined as being the maximum value of the Raman spectrum intensity, as shown in Figure 7. In general there are no crystalline constructions which exceed a .

monocrystalline silicon wafer, and therefore the maximum value of the Raman intensity shown on the vertical axis in Figure 4 is 1. It can be seen that as the value of the Raman intensity approaches 1, the construction approaches a monocrystalline construction.

Figure 5 shows plots of the relationship between the full-width at half magnitude for the Raman spectrum and the energy density of the laser light irradiation for samples heated to different temperatures. The full-width at half magnitude shown on the vertical axis is a parameter indicating the ratio (W/W_0) between the width W_0 of the spectrum at a position at half of the Raman spectrum intensity for a monocrystalline silicon wafer and the width W of the spectrum at a position at half of the Raman spectrum intensity which was actually obtained for the sample. W and W_0 are defined as the width of the spectrum at a position of half of the Raman spectrum intensity, as shown in Figure 7. In general, a narrow, sharp Raman spectrum means that the crystallinity is excellent. Consequently, in general the width of the Raman spectrum for monocrystalline silicon is the thinnest and the sharpest. It should be noted that the samples which were used were the same as those for which the data shown in Figure 4 was obtained.

Thus the full-width at half magnitude shown in Figure 5 is generally a value of 1 or more. It can further be seen that as the value approaches 1, the construction approaches a monocrystalline construction. As can be seen from Figure 5, it is possible to obtain a crystallinity which approaches that of a monocrystal if the temperature to which the sample is heated during irradiation with laser light is increased. It can further be seen that the effects due to heating the sample become saturated at about 500°C.

It can be concluded from Figure 5 that in order to obtain stable crystallinity which approaches that of a monocrystal, heating to 400°C is not reliable, and it is therefore preferable to heat to 450°C or more in order to provide some leeway.

In the opinion of the present inventors, a region can be regarded as being monocrystalline if the Raman intensity shown in Figure 4 is 0.8 or more, the full-width at half magnitude of the Raman spectrum shown in Figure 5 is 2.0 or less, and there are effectively no crystal grain boundaries within the region.

The region which can be regarded as being monocrystalline is one in which a silicon film formed by the plasma CVD method or the reduced pressure thermal CVD method is used as the starting film, and the film contains carbon and nitrogen at a concentration of between 1×10^{16} and $5 \times 10^{18} \text{ cm}^{-3}$ and oxygen at a concentration of between 1×10^{17} and $5 \times 10^{19} \text{ cm}^{-3}$. Further, lattice defects are present in principle, and therefore hydrogen is contained at a concentration of between 1×10^{17} and $5 \times 10^{20} \text{ cm}^{-3}$ in order to neutralize unpaired bonds in the silicon. In other words a characteristic of the region which can be regarded as being monocrystalline is that although it has point defects it does not have linear defects or surface defects. It should be noted that the concentrations of elements which are contained is defined as being the minimum value as measured by SIMS (secondary ion mass spectroscopy).

The abovementioned region which can be regarded as being monocrystalline is different from a general monocrystalline wafer. This results from its being a thin-film semiconductor with a thickness of between approximately 200 and 2000 Å which is formed by the CVD method.

The construction of another invention is

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a semiconductor device which employs a thin-film silicon semiconductor which is formed on a substrate which has an insulating surface, wherein

the abovementioned thin-film silicon semiconductor has a region which can be regarded as being effectively monocrystalline,

the abovementioned region constitutes at least part of an active layer,

and the abovementioned region contains carbon and nitrogen atoms at a concentration of between $1 \times 10^{16} \text{ cm}^{-3}$ and $5 \times 10^{18} \text{ cm}^{-3}$, and oxygen at a concentration of between $1 \times 10^{17} \text{ cm}^{-3}$ and $5 \times 10^{19} \text{ cm}^{-3}$.

The construction of another invention is

a semiconductor device which employs a thin-film silicon semiconductor which is formed on a substrate which has an insulating surface, wherein

the abovementioned thin-film silicon semiconductor has a region which can be regarded as being effectively monocrystalline,

the abovementioned region constitutes at least part of an active layer,

and the abovementioned region contains hydrogen atoms, which neutralize the unpaired bonds in the silicon, at a concentration of between $1 \times 10^{17} \text{ cm}^{-3}$ and $5 \times 10^{20} \text{ cm}^{-3}$.

The construction of another invention is

a semiconductor device which employs a thin-film silicon semiconductor which is formed on a substrate which has an insulating surface, wherein

the abovementioned thin-film silicon semiconductor has a region which can be regarded as being effectively monocrystalline,

the abovementioned region constitutes at least part of an active layer,

the abovementioned region contains carbon and nitrogen atoms at a concentration of between $1 \times 10^{16} \text{ cm}^{-3}$ and $5 \times 10^{18} \text{ cm}^{-3}$, oxygen atoms at a concentration of between $1 \times 10^{17} \text{ cm}^{-3}$ and $5 \times 10^{19} \text{ cm}^{-3}$, and hydrogen atoms, which neutralize the unpaired bonds in the silicon, at a concentration of between $1 \times 10^{17} \text{ cm}^{-3}$ and $5 \times 10^{20} \text{ cm}^{-3}$,

and the thickness of the abovementioned thin-film silicon semiconductor is on average between 200 and 2000 Å.

The construction of another invention is

a semiconductor device which employs a thin-film silicon semiconductor which is formed on a substrate which has an insulating surface, wherein

a region of the abovementioned thin-film silicon semiconductor which has a crystalline construction which can be regarded as being effectively monocrystalline constitutes at least a channel-forming region,

and the abovementioned channel-forming region contains carbon and nitrogen atoms at a concentration of between $1 \times 10^{16} \text{ cm}^{-3}$ and $5 \times 10^{18} \text{ cm}^{-3}$, oxygen atoms at a concentration of between $1 \times 10^{17} \text{ cm}^{-3}$ and $5 \times 10^{19} \text{ cm}^{-3}$, and hydrogen atoms, which neutralize the unpaired bonds in the silicon, at a concentration of between $1 \times 10^{17} \text{ cm}^{-3}$ and $5 \times 10^{20} \text{ cm}^{-3}$.

The construction of another invention is

a method of fabricating a semiconductor device, which method comprises a step in which a region which can be regarded as being monocrystalline is formed by irradiating with laser light a silicon thin film which is formed on a substrate which has an insulating surface,

wherein the abovementioned laser light irradiation is performed in a state in which the sample has been heated to a temperature of between 450°C and 750°C .

The construction of another invention is

a semiconductor device which has a construction in which a plurality of thin-film transistors are connected in parallel,

and each of the abovementioned plurality of thin-film transistors has a construction in which there are effectively no crystal grain boundaries within the channel-forming region.

The construction of another invention is

a semiconductor device which has a construction in which a plurality of thin-film transistors are connected in parallel,

each of the abovementioned plurality of thin-film transistors has a construction in which there are effectively no crystal grain boundaries within the channel-forming region,

and the abovementioned channel-forming region contains carbon and nitrogen atoms at a concentration of between $1 \times 10^{16} \text{ cm}^{-3}$ and $5 \times 10^{18} \text{ cm}^{-3}$, oxygen atoms at a concentration of between $1 \times 10^{17} \text{ cm}^{-3}$ and $5 \times 10^{19} \text{ cm}^{-3}$, and hydrogen atoms, which neutralize the unpaired bonds in the silicon, at a concentration of between $1 \times 10^{17} \text{ cm}^{-3}$ and $5 \times 10^{20} \text{ cm}^{-3}$.

The construction of another invention is

a semiconductor device which has a construction in which a plurality of thin-film transistors are connected in parallel,

each of the abovementioned plurality of thin-film transistors has a construction in which there are effectively no crystal grain boundaries within the channel-forming region,

the abovementioned channel-forming region has a thickness of between 200 and 2000 Å,

and the abovementioned channel-forming region

contains carbon and nitrogen atoms at a concentration of between $1 \times 10^{16} \text{ cm}^{-3}$ and $5 \times 10^{18} \text{ cm}^{-3}$, oxygen atoms at a concentration of between $1 \times 10^{17} \text{ cm}^{-3}$ and $5 \times 10^{19} \text{ cm}^{-3}$, and hydrogen atoms, which neutralize the unpaired bonds in the silicon, at a concentration of between $1 \times 10^{17} \text{ cm}^{-3}$ and $5 \times 10^{20} \text{ cm}^{-3}$.

The construction of another invention is

a semiconductor device which has a construction in which a plurality of thin-film transistors are connected in parallel,

and each of the abovementioned plurality of thin-film transistors is constructed from a thin-film silicon semiconductor in which the channel-forming region can be regarded as being effectively monocrystalline.

By constructing a thin-film transistor using, as the active layer, a region of a thin-film semiconductor transistor which region can be regarded as being monocrystalline, it is possible to obtain a thin-film transistor which has high voltage resistance and in which there is no variation or degradation of characteristics.

Further, by adopting a construction in which there are connected in parallel a plurality of thin-film transistors which are constructed using, as the active region, a region of a thin-film silicon semiconductor which region can be regarded as being monocrystalline, it is possible to obtain a construction with which it is possible to allow a large current to flow. With such constructions it is possible to obtain effects which are effectively the same as those obtained by increasing the channel width. By adopting this construction it is possible to obtain the same characteristics as with a transistor which is formed using a semiconductor which can be regarded as being monocrystalline, and it is possible to obtain a large

mobility, a large voltage resistance and stabilized characteristics.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1(A) to 1(D) show the fabrication steps of an embodiment of a thin-film transistor.

Figure 2(A) to 2(D) show the fabrication steps of an embodiment of a thin-film transistor.

Figure 3 shows the construction of an embodiment of a thin-film transistor.

Figure 4 shows the relationship between the energy density of laser light irradiation and the Raman intensity for cases in which the temperature to which the sample is heated varies.

Figure 5 shows the relationship between the energy density of laser light irradiation and the full-width at half magnitude of the Raman spectrum for cases in which the temperature to which the sample is heated varies.

Figure 6 shows an example of a liquid crystal electrooptical device which is integrated on a single substrate.

Figure 7 shows an example of a Raman spectrum.

Figure 8 shows the construction of an embodiment of a thin-film transistor.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[Embodiment 1]

The present embodiment employs a glass substrate (Corning 7059) as the substrate, and is an example in which a thin-film transistor is fabricated at a temperature which is lower than the distortion temperature of the glass substrate. The distortion temperature of Corning 7059 glass is 593°C, and therefore heat treatments at temperatures above this temperature are not preferable since they give

rise to shrinkage and deformation of the glass substrate. In particular, if use is made of a glass substrate which has a large surface area, for use in a particularly large liquid crystal display device, shrinkage and deformation of the glass substrate have significant effects.

Thus the thin-film transistor shown in the present embodiment is characterized in that the effects of heat on the substrate are greatly reduced by the maximum temperature in the heat treatment step being 600°C or less, and preferably 550°C or less.

Figure 1 shows the fabrication steps for the thin-film transistor given in the present embodiment. Firstly, a silicon oxide film 102 is formed by the sputtering method to a thickness of 3000 Å on a quartz substrate 101 as a base film. An amorphous silicon film 103 is then formed by the plasma CVD method or the low-pressure thermal CVD method to a thickness of 500 Å. (Figure 1 (A))

After forming the amorphous silicon film 103, heat treatment is performed at a temperature of 600°C, thereby crystallizing the amorphous silicon film 103. Laser light is then irradiated, crystal growth is effected centered on the region indicated by 104, and a crystalline region 106 which can be regarded as being monocrystalline is obtained. The laser light irradiation is performed while the sample or surface being irradiated is heated to a temperature of 600°C. The laser light irradiation is performed in the region indicated by 104 in Figure 1, and at this time crystal growth proceeds outwards from the region indicated by 104. (Figure 1 (A))

In the abovementioned step, it is advantageous to introduce into the amorphous silicon film a metal element which promotes crystallization. In this way it is possible to form a region which can be regarded as being

monocrystalline over a larger surface area.

Having obtained the region 106 which can be regarded as being monocrystalline, the active layer of the thin-film transistor is formed by patterning, using this region. Most preferably the whole of the active layer is formed within the region which can be regarded as being monocrystalline. However, depending on the size of the active layer, there are cases in which the resulting monocrystalline region is relatively small, and it is difficult to construct the whole of the active layer. In these cases it is possible to arrange that there are no crystal grain boundaries within the channel-forming region by making the channel-forming region the region which can be regarded as being monocrystalline.

Having formed the active layer, a silicon oxide film 107 is formed as a gate insulating film to a thickness of 1000 Å using the plasma CVD method. A film whose main component is aluminum, containing 0.2% scandium, is then formed to a thickness of 6000 Å. A gate electrode 108 is then obtained by patterning the film whose main component is aluminum.

An oxide layer 109 is then formed by performing anodic oxidation using the gate electrode 108 as the anode, in an ethylene glycol solution containing 10% tartaric acid. The thickness of the oxide layer 109 is approximately 2000 Å. Due to the presence of the oxide layer it is possible to form offset gate regions in the subsequent step in which impurity ions are injected.

Impurity ions, phosphorus ions for an N-channel type thin-film transistor, or boron ions for a P-channel type thin-film transistor, are then injected into the active layer. In this step, the gate electrode 108 and the oxide layer 109 at the periphery thereof act as a mask, and

impurity ions are injected into the regions indicated by 110 and 114. The region 110 in which impurity ions have been injected then forms the source region, and the region 114 forms the drain region. Further, the oxide layer 109 at the periphery of the electrode 108 acts as a mask, and offset gate regions 111 and 113 are formed simultaneously. Further, a channel-forming region 112 is also formed in a self-aligning manner. (Figure 1 (C))

After completion of the impurity ion injection step, laser light is irradiated, thereby annealing the active layer which was damaged by the injection of the impurity ions, and activating the injected impurities. This step may also be performed by irradiating with strong light such as infrared light.

Further, a silicon oxide film 115 is formed to a thickness of 7000 Å by the plasma CVD method as a layer insulating film. After passing through a hole-opening step, a source electrode 116 and a drain electrode 117 are formed. Further, by performing heat treatment in a hydrogen atmosphere at 350°C the thin-film transistor is completed. (Figure 1 (D))

In the thin-film transistor shown in the present embodiment, the active layer is constructed from a region which has a construction which can be regarded as being monocrystalline, and it is therefore possible to solve the problems of low voltage resistance resulting from crystal grain boundaries, and the problem of a large leak current.

[Embodiment 2]

The present embodiment indicates an example in which a thin-film transistor is constructed using a crystalline region which can be regarded as being monocrystalline, said region being formed by introducing into an amorphous silicon film a metal element which promotes crystallization.

Figure 2 shows the fabrication steps in the present embodiment. Firstly, a silicon oxide film 102 is formed to a thickness of 3000 Å by the sputtering method on a glass substrate 101 as a base film. An amorphous silicon film 103 is then formed to a thickness of 1000 Å by the plasma CVD method or the reduced-pressure thermal CVD method. An extremely thin oxide film (not shown) is then formed on the surface of the amorphous silicon film by the UV oxidation method. This oxide film is intended to improve solution wetting in the subsequent solution application step. The UV oxidation step which is performed here involves irradiation with UV light in an oxidizing atmosphere, thereby forming an extremely thin oxide film on the surface of the surface which is being irradiated.

A nickel acetate solution is then coated by the spin coating method onto the surface of the amorphous silicon film 103 on which is formed the extremely thin oxide film, thereby forming a film 100 containing nickel. Due to the presence of the film 100, the nickel element is disposed in contact with the amorphous silicon film via the extremely thin oxide film.

In this state the amorphous silicon film 103 is transformed into a crystalline silicon film by subjecting it to heat treatment at 550°C for 4 hours. Here, since nickel, which is a metal element which promotes crystallization, has been introduced, it is possible to obtain a crystalline silicon film by heat treating at 550°C for approximately 4 hours.

Having obtained the silicon film 103 which has been transformed into a crystalline silicon film by heat treatment, crystal growth is effected from the region indicated by 104 in Figure 2 by irradiating with laser light. In the present embodiment, nickel, which is a metal

element which promotes crystallization, has been introduced, and it is therefore possible to obtain a region which can be regarded as being monocrystalline, as indicated by 106, simply.

Having thus obtained the region 106 which can be regarded as being monocrystalline, as indicated in Figure 2 (B), the active layer of the thin-film transistor is formed using this region. Further, the film containing nickel is removed before or after formation of the active layer.

Having formed the active layer, a gate insulating layer 107 is constructed from a silicon oxide film, and furthermore a gate electrode 108 whose main component is aluminum, and an oxide layer 109 at the periphery thereof are formed. These fabrication steps are the same as indicated in embodiment 1.

Having obtained the state shown in Figure 2 (C) in this way, impurity ions are injected, and a source region 110 and a drain region 114 are formed. In this step, offset gate regions 111 and 113, and also a channel-forming region 112 are formed in a self-aligning manner.

Furthermore, by irradiating with laser light, damage caused when the impurity ions were injected is annealed, and impurity ions which have been injected are activated.

A silicon oxide film 115 is then formed as a layer insulating film by the plasma CVD method, and after passing through a hole-opening step, a source electrode 116 and a drain electrode 117 are formed. Finally, by heat treating for 1 hour in a hydrogen atmosphere at 350°C, the thin-film transistor shown in Figure 2 (D) is completed.

[Embodiment 3]

The present embodiment relates to a construction in which the inventions disclosed in the present specification are employed in a thin-film transistor which is required to

handle large currents. For example, in the peripheral circuitry of an active matrix-type liquid crystal display device, a buffer amplifier (a power conversion circuit which has a low output impedance) through which large currents can flow is required in order to drive the many thousands of pixel transistors which are provided. For cases in which not only the display region but also the peripheral circuitry region is to be integrated on a single substrate, there is the need to construct the buffer amplifier using thin-film transistors.

In order to construct a thin-film transistor which can be used in such a buffer amplifier, it is necessary for the channel-forming region of the thin-film transistor to have a width of several tens of micrometers or more. However, if crystalline silicon thin films which have a general multicrystalline or microcrystalline construction are used, the voltage resistance is low, and there are problems in that it is difficult to construct the required buffer amplifier. Further, when high speed operations are performed, there is the problem that variations and drift of the characteristics are liable to occur. This is due to the fact that the threshold value in each transistor varies, and characteristics are likely to be degraded. Further, there are serious problems of heat generation, and there are also problems in that the characteristics are degraded by the effects of heat generation. The main reason for these problems is that crystal grain boundaries exist within the active layer (in particular within the channel-forming region).

Thus the present embodiment provides a construction in which there are connected in parallel a plurality of thin-film transistors in each of which the channel-forming region is constructed using a region which can be regarded

as being monocrystalline, and with which it is possible to handle currents of a size similar to thin-film transistors which have an equivalently large channel width.

Figure 3 shows the construction of a thin-film transistor indicated in the present embodiment. The construction given in the present embodiment shows a construction in which three thin-film transistors are connected in parallel. The construction shown in Figure 3 is a construction in which the active layer forming the channel-forming region and periphery thereof in each thin-film transistor is constructed from a silicon semiconductor thin-film which can be regarded as being monocrystalline.

In Figure 3, the regions indicated by 106 are regions which can be regarded as being monocrystalline. The regions which can be regarded as being monocrystalline, indicated by 106, include part of the channel-forming region and source/drain regions. It is therefore possible to construct not only the channel-forming region, but also the interface between the source region and the channel-forming region and the vicinity thereof, and the interface between the drain region and the channel-forming region and the vicinity thereof such that they can be regarded as being monocrystalline.

When such a construction is adopted, it is possible to solve the problems which arise due to the presence of crystal grain boundaries. In other words, it is possible to solve the problem of low voltage resistance, the problem of degradation of characteristics and the problem of variations in threshold values. Further, since it is possible to reduce the number of carriers which migrate between the source and drain via the crystal grain boundaries it is possible to reduce the off current.

The cross section through A-A1 of the construction shown in Figure 3 corresponds to Figure 1 (D). In other words, the construction shown in Figure 3 has a construction in which three thin-film transistors shown in Figure 1 (D) are connected in parallel. Each transistor has a common gate electrode, and the source electrode and drain electrode are wired in common by contacts 305 and 306.

If the construction shown in the present embodiment is adopted, it is possible to perform operations equivalent to using a thin-film transistor which has a channel width of 60 μm , even though the channel width of each thin-film transistor is 20 μm , by connecting three thin-film transistors in parallel.

The present embodiment shows an example in which three thin-film transistors are connected in parallel. However, the number of thin-film transistors which are connected in parallel can be selected as necessary.

By adopting a construction such as shown in the present embodiment it is possible to obtain a thin-film transistor which has characteristics which are similar to a thin-film transistor which employs a semiconductor which can be regarded as being monocrystalline, and which can handle large currents. It is therefore possible to perform high speed operations, and it is furthermore possible to achieve a construction with which there is no degradation or variation of characteristics.

The construction shown in the present embodiment can be said to be ideal for circuits which require a large current to flow, for example buffer circuits which are provided in the peripheral circuitry of active matrix-type liquid display devices.

[Embodiment 4]

Figure 6 shows the architecture of a high-accuracy active matrix liquid crystal display system which employs the invention disclosed in the present specification. The example shown in Figure 6 is an example which has been made small, lightweight and thin by fixing semiconductor chips which are normally attached to the main board of a computer onto at least one of the substrates of a liquid crystal display which has a construction in which liquid crystal is sandwiched between a pair of substrates.

A description of Figure 6 will now be given. The substrate 15 is a substrate of a liquid crystal display, and an active matrix circuit 14 which is formed from a number of pixels which are provided with a TFT 11, a pixel electrode 12 and an auxiliary capacitor 13, an X decoder/driver, a Y decoder/driver and an XY branching circuit are formed on the substrate 15 using TFTs. In order to drive the active matrix circuit, a buffer circuit which has a low output impedance must be provided in the peripheral circuit, and this buffer circuit is advantageously constructed using a circuit such as shown in Figure 3.

Other chips are also attached to the substrate 15. These chips are connected to the circuitry on the substrate 15 by a means such as the wire bonding method or the COG (chip on glass) method. In Figure 6, the chips which are attached in this way are the correction memory, the memory, the CPU and the input board, but various other chips may also be attached.

In Figure 6, the input board is a circuit which reads signals which have been input from outside, and converts them into image signals. The correction memory is a memory which is unique to the active matrix panel and is used to correct input signals and the like in order to match them to the characteristics of the panel. In particular, the

correction memory uses nonvolatile memory for information unique to each pixel, and corrects them individually. In other words, if there is a point defects in a pixel of an electrooptical device then signals are sent to pixels around this point to match with it, thereby covering the point defect such that the defect is not noticeable. Further, if a pixel is darker than the surrounding pixels then a larger signal is sent to that pixel such that it has the same brightness as the surrounding pixels. The defect information for pixels is different for each panel, and therefore the information stored in the correction memory is different for each panel.

The functions of the CPU and memory are the same as for a normal computer, and in particular memory is provided as RAM for the image memory corresponding to each pixel. All of these chips are CMOS type.

It is further possible to increase the thin film of the system by constructing at least part of the required integrated circuits using the inventions disclosed in the present specification.

In this way, forming even the CPU and memory on the liquid crystal display substrate, and constructing an electronic device such as a simple personal computer on a single substrate is extremely advantageous in reducing the size of liquid crystal display systems and widening their scope of application.

It is possible to use the thin-film transistors fabricated using the inventions disclosed in the present specification for circuits which are required in systemized liquid crystal displays. In particular, it is extremely advantageous to use thin-film transistors fabricated using regions which can be regarded as being monocrystalline in analog buffer circuits or other necessary circuits.

[Embodiment 5]

The present embodiment relates to a construction in which three thin-film transistors are connected in parallel as shown in Figure 8. In Figure 8, 804 indicates a common active layer, and 803 is a region which can be regarded as being monocrystalline and which is formed in the active layer. In Figure 8, three regions which can be regarded as being monocrystalline are shown, and the channel-forming regions of each thin-film transistor are formed in the three regions which can be regarded as being monocrystalline.

801 is a common gate electrode and gate wiring. 805 is a common source electrode and source wiring. 806 is a common drain electrode and drain wiring. Further, 802 indicates contact portions between the source/drain electrodes and the source/drain regions.

By employing the inventions disclosed in the present specification it is possible to obtain a thin-film transistor which is not affected by crystal grain boundaries. It is further possible to obtain a thin-film transistor which has high voltage resistance and with which there is no variation in characteristics, and with which it is possible to handle large currents. Further, since it is possible for the operation of the thin-film transistor not to be affected by crystal grain boundaries, it is possible for the off current to have a small characteristic.

WHAT IS CLAIMED IS:

1. An electro-optical device comprising:
 - at least two transistors provided on an insulating surface;
 - a common gate wiring provided on said insulating surface and
 - 5 connected with said two transistors at gate electrodes of said two transistors;
 - a common source wiring provided on said insulating surface
 - and connected with said two transistors at one of source and drain of each
 - of said two transistors; and
 - a common drain wiring provided on said insulating surface
 - 10 and connected with said two transistors at the other of the source and drain
 - of each of said two transistors,
 - wherein said two transistors are connected with each other in
 - parallel by the connections of said common gate wiring, said common
 - source wiring and said common drain wiring with said two transistors,
 - 15 wherein at least channel-forming regions of said at least two
 - transistors are provided in regions which can be regarded as being
 - effectively monocrystalline, and
 - wherein said regions which can be regarded as being
 - effectively monocrystalline comprise silicon.
- 20 2. An electro-optical device comprising:
 - at least two transistors provided on an insulating surface in a
 - peripheral circuitry of said electro-optical device;
 - a common gate wiring provided on said insulating surface and
 - connected with said two transistors at gate electrodes of said two transistors;

a common source wiring provided on said insulating surface and connected with said two transistors at one of source and drain of each of said two transistors; and

5 a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors,

10 wherein at least channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline, and

wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

15 3. An electro-optical device comprising:

at least two transistors provided on an insulating surface in a buffer circuit of a peripheral circuitry of said electro-optical device;

a common gate wiring provided on said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

20 a common source wiring provided on said insulating surface and connected with said two transistors at one of source and drain of each of said two transistors; and

a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain
25 of each of said two transistors,

wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors,

5 wherein at least channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline, and

wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

4. An electro-optical device comprising:

10 an active matrix circuit provided on an insulating surface;
at least two transistors provided on said insulating surface in a peripheral circuitry of said electro-optical device provided around said active matrix circuit;

15 a common gate wiring provided on said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

a common source wiring provided on said insulating surface and connected with said two transistors at one of source and drain of each of said two transistors; and

20 a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors,

25 wherein at least channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline, and

wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

5. An electro-optical device comprising: an active matrix circuit provided on an insulating surface;

5 at least two transistors provided on said insulating surface in a buffer circuit of a peripheral circuitry of said electro-optical device provided around said active matrix circuit;

a common gate wiring provided on said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

10 a common source wiring provided on said insulating surface and connected with said two transistors at one of source and drain of each of said two transistors; and

a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

15 wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors,

20 wherein at least channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline, and

wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

6. An electro-optical device comprising:

25 at least two transistors provided on an insulating surface;

a common gate wiring provided on said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

a common source wiring provided on said insulating surface and connected with said two transistors at one of source and drain of each of said two transistors; and

a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors,

wherein at least channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline,

wherein said channel-forming regions of said at least two transistors are separately provided in at least two separate islands respectively, and

wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

7. An electro-optical device comprising: at least two transistors provided on an insulating surface;

a common gate wiring provided on said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

a common source wiring provided on said insulating surface and connected with said two transistors at one of source and drain of each of said two transistors; and

a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

5 wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors,

wherein at least channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline,

10 wherein said channel-forming regions of said at least two transistors are provided in a common island; and

wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

8. An electro-optical device comprising:

15 at least two transistors provided on an insulating surface in a peripheral circuitry of said electro-optical device;

a common gate wiring provided on said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

20 a common source wiring provided on said insulating surface and connected with said two transistors at one of source and drain of each of said two transistors; and

a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

25 wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors,

wherein at least channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline,

5 wherein said channel-forming regions of said at least two transistors are separately provided in at least two separate islands respectively, and

wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

9. An electro-optical device comprising: at least two transistors
10 provided on an insulating surface in a peripheral circuitry of said electro-optical device;

a common gate wiring provided on said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

15 a common source wiring provided on said insulating surface and connected with said two transistors at one of source and drain of each of said two transistors; and

a common drain wiring provided on said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

20 wherein said two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said two transistors,

25 wherein at least channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline,

wherein said channel-forming regions of said at least two transistors are provided in a common island; and

wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

10. An electro-optical device which employs a thin-film semiconductor which is formed on an insulating surface, wherein

5 the thin-film semiconductor has a region which can be regarded as being effectively monocrystalline,

the region contains carbon and nitrogen atoms at a concentration of $5 \times 10^{18} \text{ cm}^{-3}$ or less, oxygen atoms at a concentration of $5 \times 10^{19} \text{ cm}^{-3}$ or less, and

10 wherein the region constitutes at least part of a channel-forming region.

11. The device of claim 1 wherein said electro-optical device has a memory.

12. The device of claim 1 wherein said electro-optical device has
15 a decoder.

13. The device of claim 1 wherein said electro-optical device is a display system.

14. The device of claim 2 wherein said electro-optical device has a memory.

20 15. The device of claim 2 wherein said electro-optical device has a decoder.

16. The device of claim 2 wherein said electro-optical device is a display system.

17. The device of claim 3 wherein said electro-optical device has a memory.

5 18. The device of claim 3 wherein said electro-optical device has a decoder.

19. The device of claim 3 wherein said electro-optical device is a display system.

10 20. The device of claim 4 wherein said electro-optical device has a memory.

21. The device of claim 4 wherein said electro-optical device has a decoder.

22. The device of claim 4 wherein said electro-optical device is a display system.

15 23. The device of claim 5 wherein said electro-optical device has a memory.

24. The device of claim 5 wherein said electro-optical device has a decoder.

25. The device of claim 5 wherein said electro-optical device is a display system.

26. The device of claim 6 wherein said electro-optical device has a memory.

5 27. The device of claim 6 wherein said electro-optical device has a decoder.

28. The device of claim 6 wherein said electro-optical device is a display system.

10 29. The device of claim 7 wherein said electro-optical device has a memory.

30. The device of claim 7 wherein said electro-optical device has a decoder.

31. The device of claim 7 wherein said electro-optical device is a display system.

15 32. The device of claim 8 wherein said electro-optical device has a memory.

33. The device of claim 8 wherein said electro-optical device has a decoder.

34. The device of claim 8 wherein said electro-optical device is a display system.

35. The device of claim 9 wherein said electro-optical device has a memory.

5 36. The device of claim 9 wherein said electro-optical device has a decoder.

37. The device of claim 9 wherein said electro-optical device is a display system.

10 38. The device of claim 1 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

15 39. The device of claim 1 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

20 40. The device of claim 2 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

41. The device of claim 2 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

5 42. The device of claim 3 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

10 43. The device of claim 3 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

15 44. The device of claim 4 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

20 45. The device of claim 4 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

46. The device of claim 5 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

47. The device of claim 5 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

48. The device of claim 6 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

49. The device of claim 6 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

50. The device of claim 7 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

51. The device of claim 7 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

5 52. The device of claim 8 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

10 53. The device of claim 8 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

15 54. The device of claim 9 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

20 55. The device of claim 9 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

56. The device of claim 10 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

57. The device of claim 10 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

ABSTRACT

Regions 106 which can be regarded as being monocrystalline are formed locally by irradiating with laser light, and at least the channel-forming region 112 is constructed using these regions. With thin-film transistors which have such a construction it is possible to obtain characteristics which are similar to those which employ monocrystals. Further, by connecting in parallel a plurality of such thin-film transistors it is possible to obtain characteristics which are effectively equivalent to those of a monocrystalline thin-film transistor in which the channel width has been increased.

064790" 9494EE60

FIG. 1A

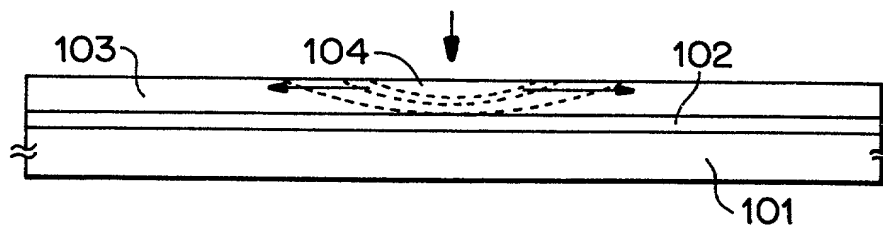


FIG. 1B

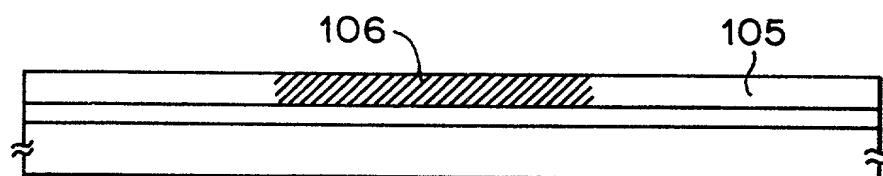


FIG. 1C

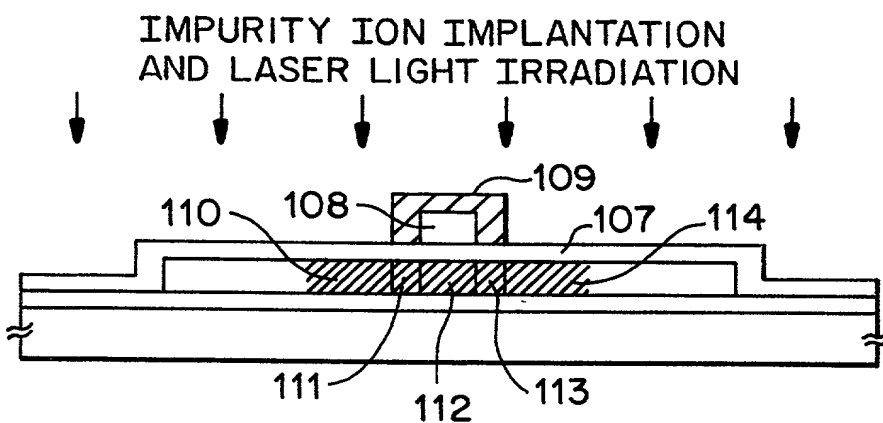
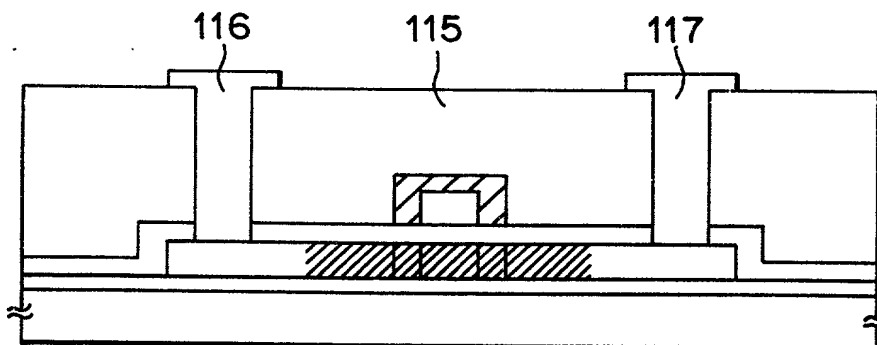


FIG. 1D



LASER LIGHT IRRADIATION

FIG. 2A

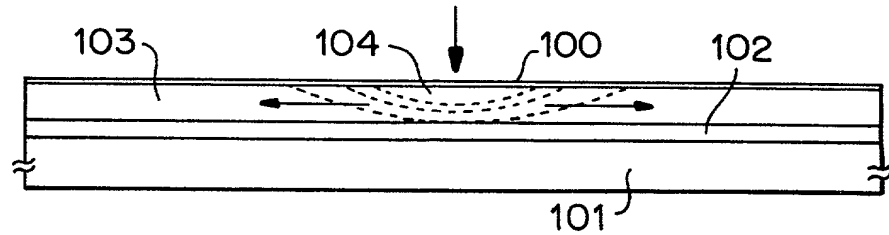
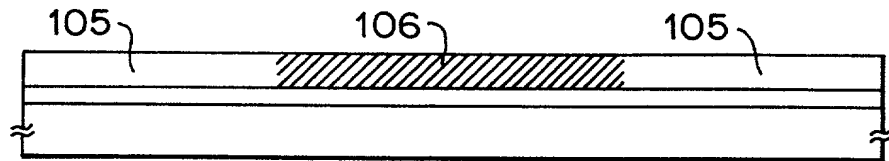


FIG. 2B



IMPURITY ION IMPLANTATION
AND LASER LIGHT IRRADIATION

FIG. 2C

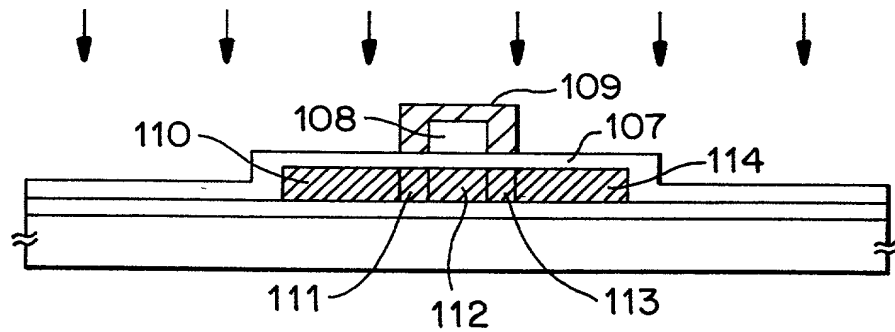


FIG. 2D

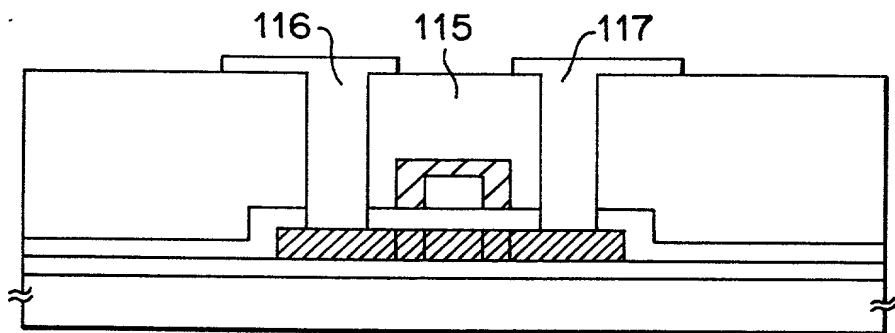


FIG. 3

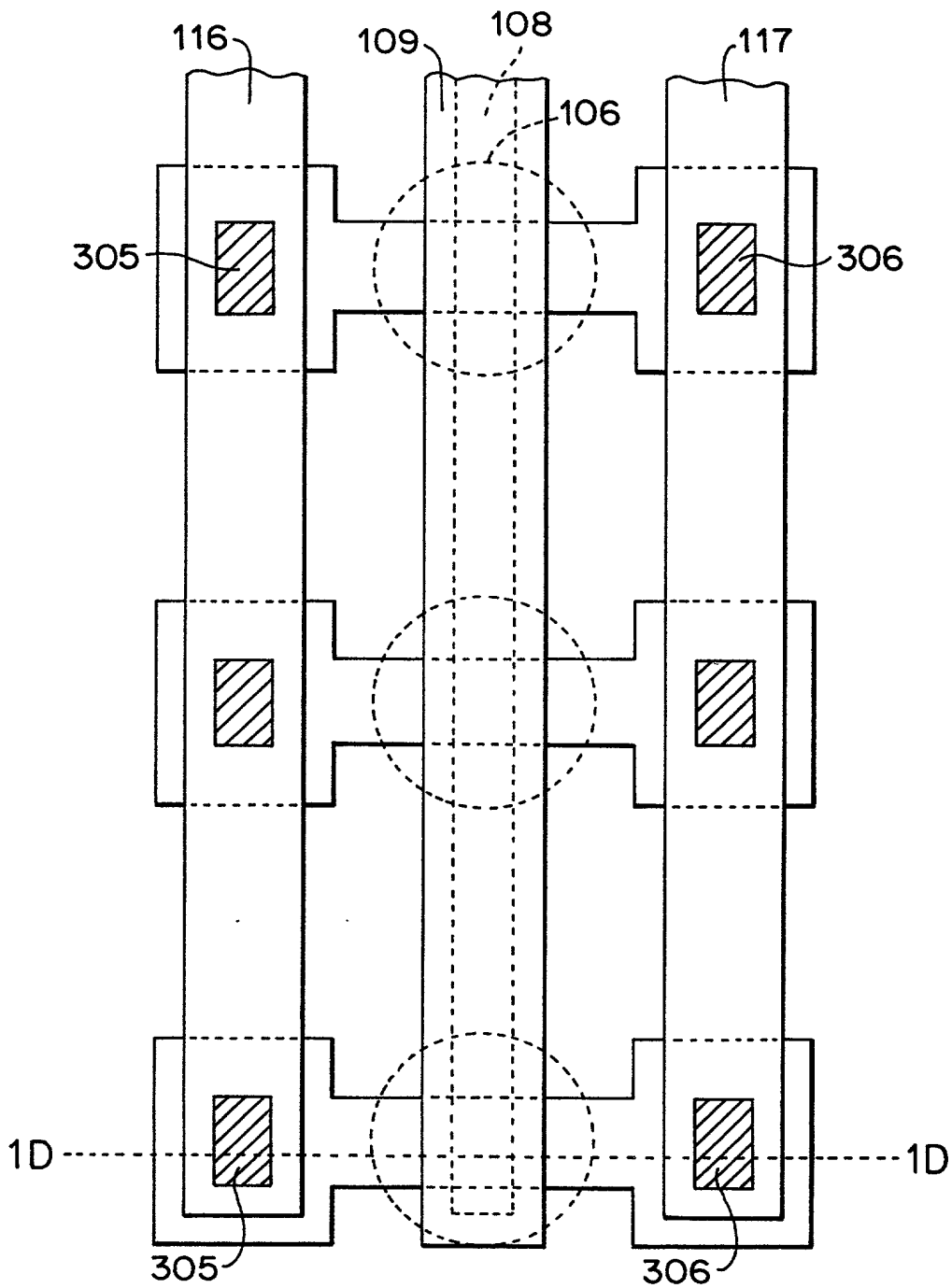


FIG. 4

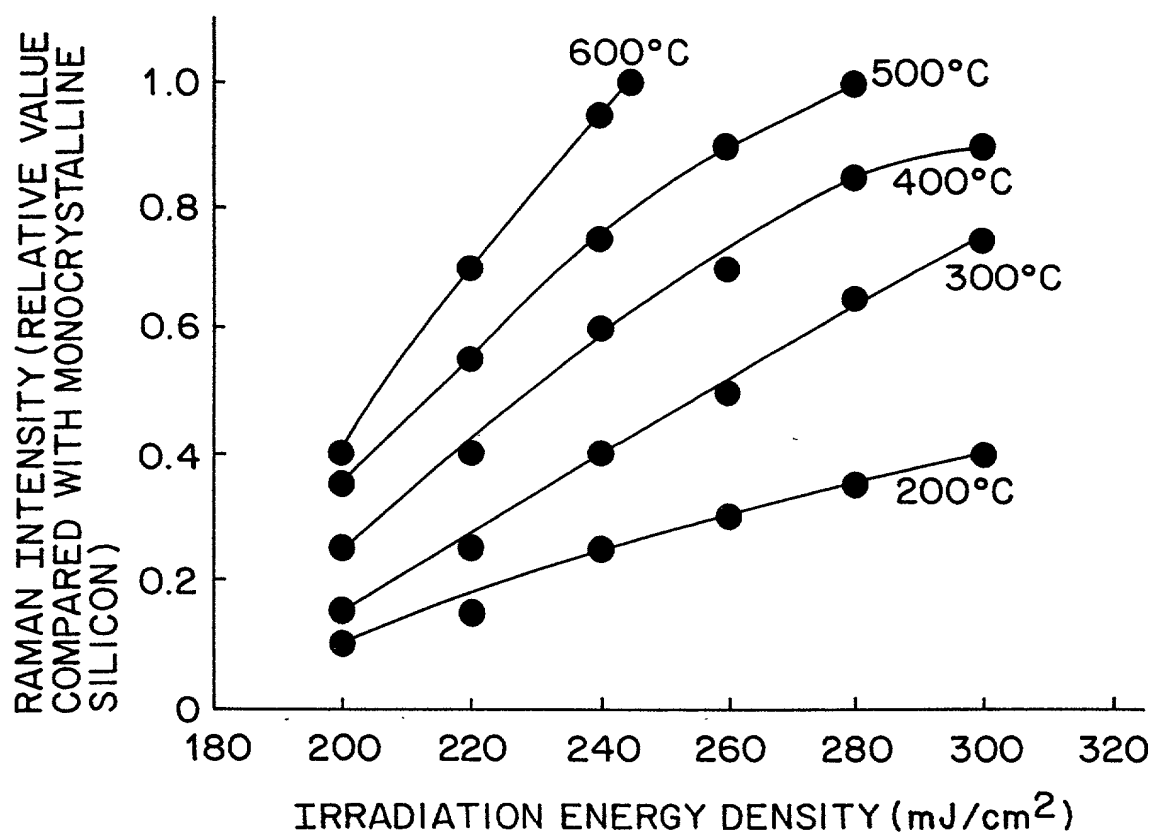


FIG. 5

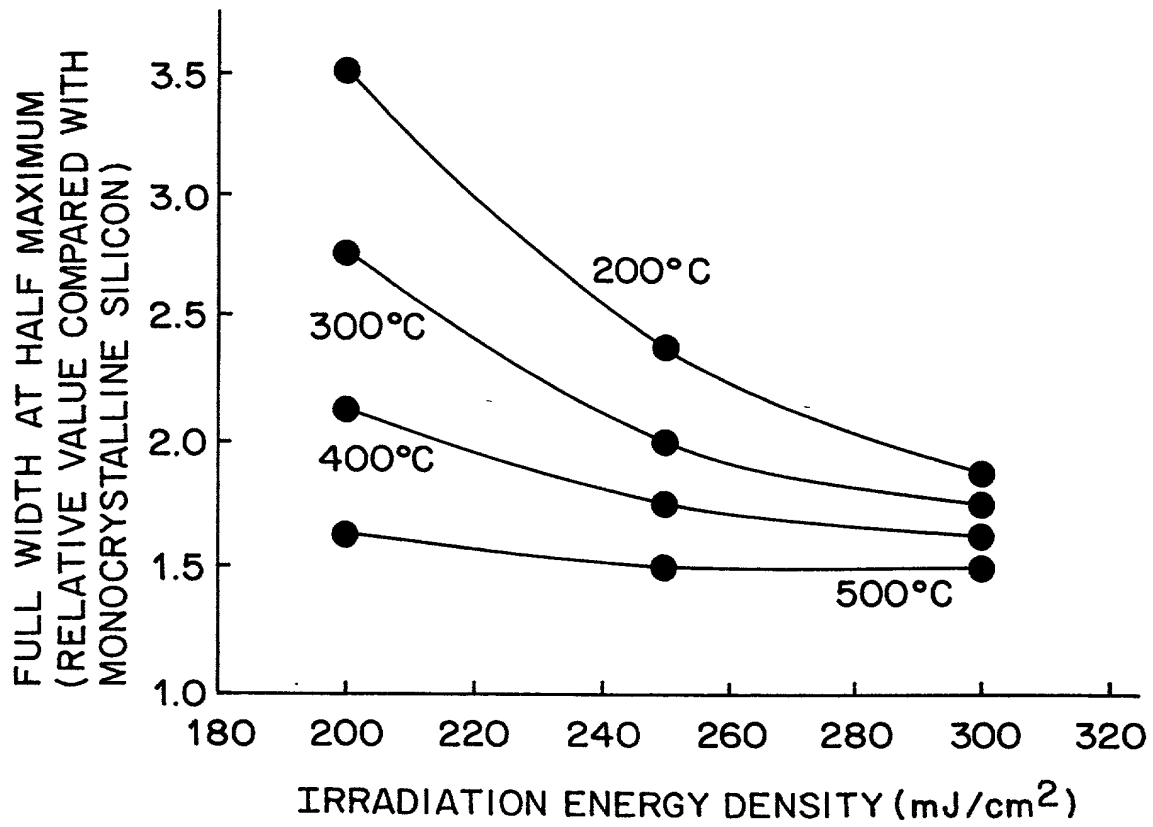


FIG. 6

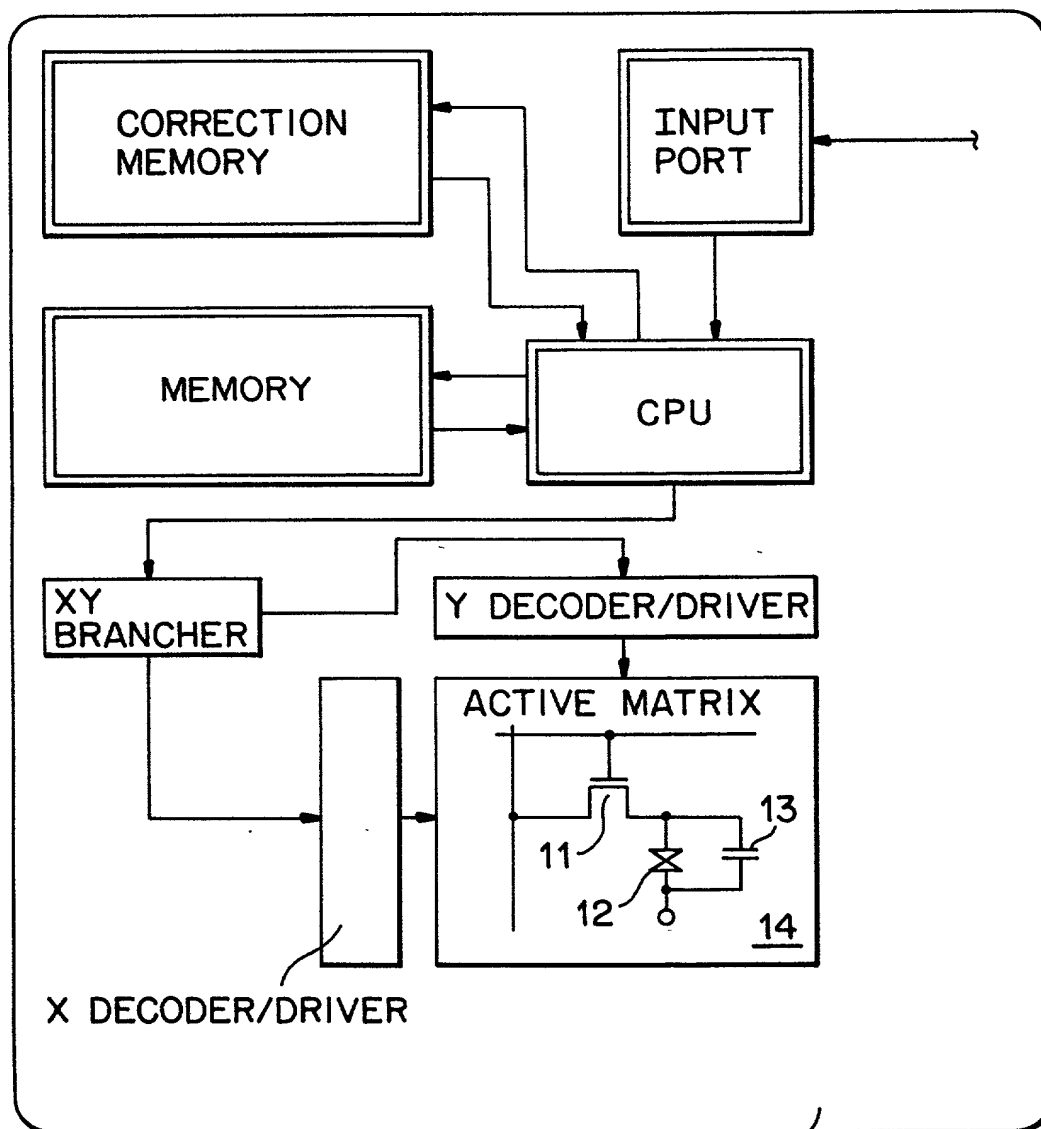


FIG. 7

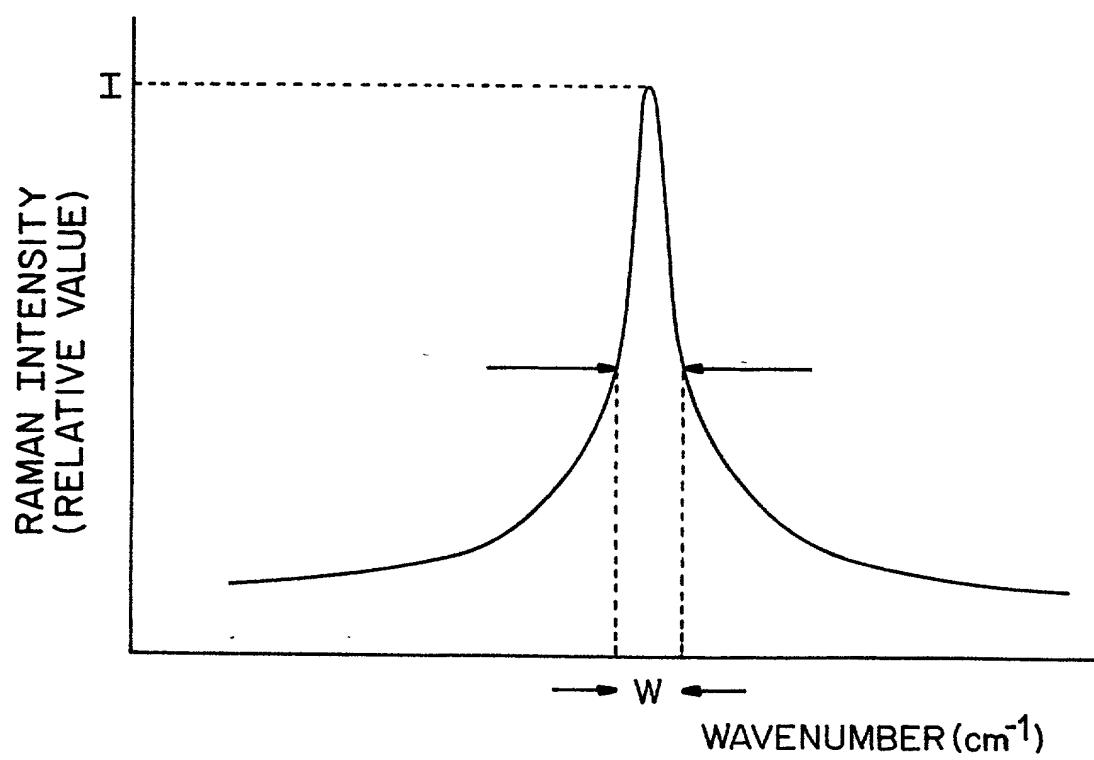
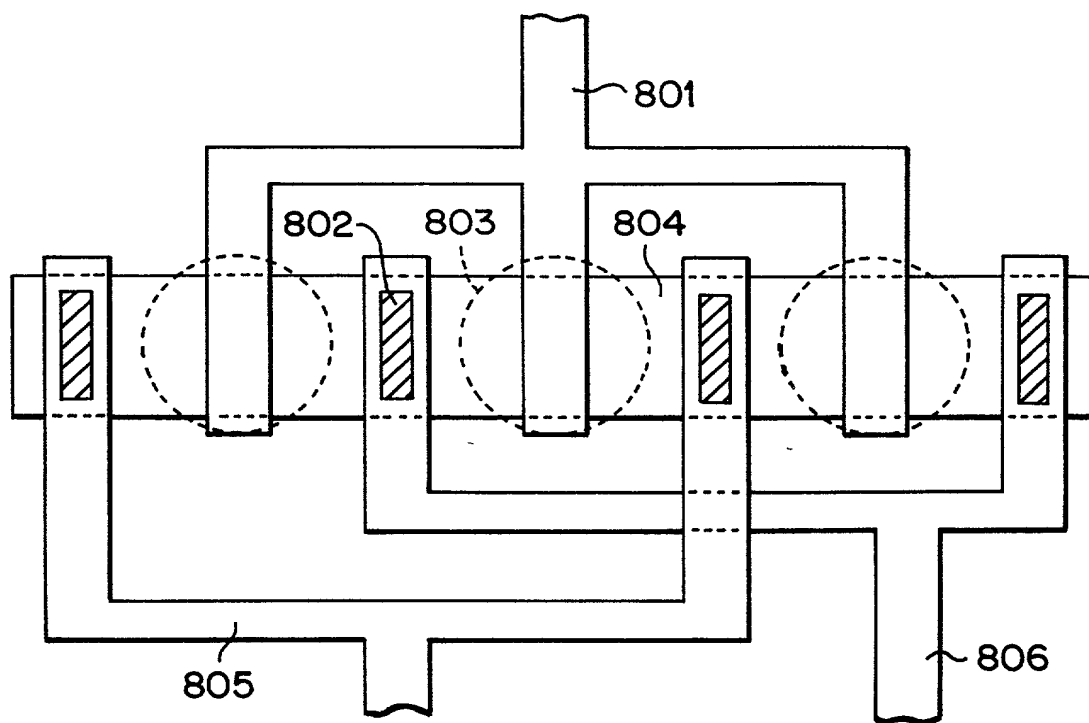


FIG. 8



DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION

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PLEASE NOTE:
YOU MUST
COMPLETE THE
FOLLOWING:

Insert Title

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the invention entitled: * Semiconductor device and fabrication
→ method thereof

→ _____, the specification
of which is attached hereto unless the following box is checked:

Check Box If
Appropriate —
For Use Without
Specification
Attached

☐ The specification was filed on _____;
and was assigned Serial No. _____
(if known)
and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof, or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as follows:

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and checked at right:

Prior Foreign Application(s)

Priority Claimed

Insert Priority
Information
(if appropriate)

| | | | | |
|----------|-----------|------------------------|---|-----------------------------|
| 6-218077 | JAPAN | August 19, 1994 | <input checked="" type="checkbox"/> Yes | <input type="checkbox"/> No |
| (Number) | (Country) | (Month/Day/Year Filed) | | |
| _____ | _____ | _____ | <input type="checkbox"/> Yes | <input type="checkbox"/> No |
| (Number) | (Country) | (Month/Day/Year Filed) | | |
| _____ | _____ | _____ | <input type="checkbox"/> Yes | <input type="checkbox"/> No |
| (Number) | (Country) | (Month/Day/Year Filed) | | |
| _____ | _____ | _____ | <input type="checkbox"/> Yes | <input type="checkbox"/> No |
| (Number) | (Country) | (Month/Day/Year Filed) | | |
| _____ | _____ | _____ | <input type="checkbox"/> Yes | <input type="checkbox"/> No |
| (Number) | (Country) | (Month/Day/Year Filed) | | |

All Foreign Applications, if any, for any Patent or Inventor's Certificate Filed More Than 12 Months Prior To The Filing Date of This Application:

| Country | Application No. | Date of Filing (Month/Day/Year) |
|---------|-----------------|---------------------------------|
| _____ | _____ | _____ |

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

| | | |
|--------------------------|---------------|---------------------------------------|
| _____ | _____ | _____ |
| (Application Serial No.) | (Filing Date) | (Status—patented, pending, abandoned) |
| _____ | _____ | _____ |
| (Application Serial No.) | (Filing Date) | (Status—patented, pending, abandoned) |

I hereby appoint the following attorneys to prosecute this application and/or an international application and to transact all business in the Patent and Trademark Office connected therewith:

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PLEASE NOTE:
 YOU MUST
 COMPLETE THE
 FOLLOWING

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

The undersigned hereby authorize any U. S. attorney or agent named herein to accept and follow instructions from _____ as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U. S. attorney or agent and the undersigned. In the event of a change in the persons from whom instructions may be taken, the U.S. attorneys or agents named herein will be so notified by the undersigned.

Insert Full Name of
 First or Sole Inventor
 and Date This
 Document Is Signed

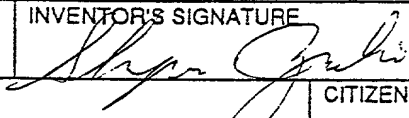
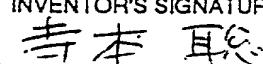
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Fourth Inventor:
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